DRIVER VOLTAGE ADJUSTER

BACKGROUND

Spatial light modulators provide an alternative technology to cathode ray tube (CRT) displays. A spatial light modulator array is an array of individually addressable elements, typically arranged in rows and columns. One or more individually addressable elements will correspond to a picture element of the displayed image.

The most prevalent spatial light modulator technology is liquid crystal displays (LCD), especially for mobile devices. In an LCD display, rows and columns of electrodes are used to orient a liquid crystalline material. The orientation of the liquid crystalline material may block or transmit varying levels of light, and is controlled by the voltages on the electrodes. These voltages are supplied to the array of elements according to the image data. A driver circuit, sometimes referred to as driver chip, performs the conversion from image data to the row and column addressing lines of the array. Given the prevalence of liquid crystal display technology, driver chips for LCD displays are widely available and marketed tested.

Unfortunately, the voltages used by many LCD driver chips have relatively fixed waveforms that limit their applicability to other types of spatial light modulator display technology that also require conversion of image data to row and column addressing line signals. In addition, it limits the availability of these widely-available driver circuits to other types of display technology.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of this invention may be best understood by reading the disclosure with reference to the drawings, wherein:

Figure 1 shows an embodiment of a display system having a display driver, a voltage adjuster and an array of modulator display elements.

Figure 2 shows a diagram of row addressing and bias signals for an interferometric modulator and a driver circuit.

Figure 3 shows a block diagram of an embodiment of a voltage adjuster.

Figure 4 shows an implementation of an embodiment of a voltage adjuster as it may be manufactured.

Figure 5 shows an embodiment of a simultaneous manufacturing process for a spatial light modulator and a voltage adjuster.

Figure 6 shows an embodiment of an adjuster network.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Figure 1 shows an embodiment of a display system 10. The standard driver circuit 12 may be one of any already commercially available flat panel display driver. As mentioned above, the most prevalent of these driver chips are those used for LCD displays. The individual display elements of an LCD array are generally defined by intersections of rows of electrodes with columns of electrodes. One method of addressing these types of arrays is known as passive array addressing.

In passive array addressing, a voltage pulse is applied a voltage pulse along one row of the electrodes while applying pulses to all of the columns. The amplitude of the column pulses corresponds to the specific data desired along the row being selected. The voltages and timing of the various pulses is such that the row being selected is the row primarily affected by the data pulses being applied to the columns.

After having written the data to the selected row, the row pulse is reduced and the next row is selected for data writing via the application of a row pulse and set of column pulses corresponding to the desired data on that row. The process is repeated in a row-by-row fashion until all of the rows have been pulsed. After pulsing every row, the sequence returns to the first row again and the process is repeated. This basic method is often used for passive matrix LCD displays. The specific waveforms used for passive matrix LCDs have evolved

over a number of years of development and have reached a relatively mature state. Generally, it is the difference in voltage between a row and a column, and the associated voltage swing, which enables the device addressing. An example of such a row addressing waveform is shown in Figure 2. As will be discussed later, embodiments of the invention may be applied to column addressing as well.

In Figure 2, the rows of the device array that are not to be addressed are held at a row bias voltage, V_{bias}. The first pulse, the one that reaches the full V_{pulse} amplitude, is that which is provided by the driver. As can be seen, the amplitude voltage swing from bias to the positive pulse has relatively large amplitude. In contrast, the positive and negative voltage pulses desired are shown by the darker lines that reach an amplitude of V_{iMoD}.

An iMoD is an example of a newer type of modulator. The iMoD employs a cavity having at least one movable or deflectable wall. As the wall, typically comprised at least partly of metal, moves towards a front surface of the cavity, interference occurs that affects the color of light viewed at the front surface. The front surface is typically the surface where the image seen by the viewer appears, as the iMoD is a direct-view device.

In a monochrome display, such as a display that switches between black and white, one iMoD element might correspond to one pixel. In a color display, three iMoD elements may make up each pixel, one each for red, green and blue.

The individual iMoD elements are controlled separately to produce the desired pixel reflectivity. Typically, a voltage is applied to the movable wall of the cavity, causing it be to electrostatically attracted to the front surface that in turn affects the color of the pixel seen by the viewer. In the display system 10 of Figure 1, a standardized driver, such as an LCD driver 12 is used with an array of interferometric modulator arrays 16 via an adjuster circuit 14. The adjuster circuit 14 adjusts the row address voltage V_{pulse} from the driver circuit 12 to an adjusted row address voltage V_{iMoD}.

An embodiment of the adjuster circuit 14 is shown in Figure 3. The adjuster circuit essential comprises a set of resistors R1 and R2, set up in a resistor divider network. The ratio of R2/R1 scales the output voltage as needed, according to the formula:

$$V_{iMoD} = \frac{R2}{R1 + R2} V_{pulse}.$$

Generally, a desirable scaling would be setting up resistors with a ratio 1:1 or 1:3. In the example of the iMoD, V_{MOD} would be V_{iMoD}. LCD drivers typically have an output range of 15-30 volts, with the desired output voltage V_{MOD} in the range of 5-15 volts. The result of applying a shunt resistor network is to reduce the amplitude of the row pulse provided by the driver, V_{pulse}, to a more acceptable level, such as V_{iMoD}.

One possible embodiment of the resistor network could be manufactured directly on the same substrate as the modulator array. On example of an exploded view of integrated metal resistors is shown in Figure 4. R1 and R2 would be manufactured out of the metal layers used in manufacturing the modulator elements. A conductive bus line 18 connects the shunt resistors R1, insulated from the input lines, preventing shorts between the shunt resistor outputs and the inputs to the modulator array. Other alternatives are of course possible. Depending upon the driver chip selected, a different level of resistance could be fabricated.

An embodiment of manufacturing an adjuster circuit simultaneously with a modulator array is shown in Figure 5. The term simultaneously as used here means that the adjuster circuit and the modulator array are both completed at the end of this process. This particular method of manufacture is for an interferometric modulator, but the implementation of the invention could occur with any modulator array that has some available area on the substrate upon which the modulator is manufactured. At 20, a first metal layer is deposited. This metal layer is then patterned and etched at 22 to form an electrode layer. An optical layer is then deposited and etched to form the active optical area of the modulator array at 24. Any area outside the active optical area could be utilized for the resistor network.

In the specific case of the iMoD, a first sacrificial layer is deposited at 26, and then a second metal layer is deposited at 28. The mirror layer is then patterned and etched at 30. In a first embodiment of this process, the patterning and etching process will also form the supports needed to suspend the mirror elements over a cavity formed when the sacrificial layer is removed. In this embodiment, the resistor is formed from the first metal layer and then connections are formed using the second metal layer. The connections cannot be formed from the same layer without an extra pattern and etch process to avoid forming a short circuit between the shunt resistor and the modulator address lines.

In an alternative embodiment, a flex layer provides a separate layer to support the mirror over the cavity. In this embodiment, a second sacrificial layer is deposited at 32. A third metal layer is deposited on the second sacrificial layer at 34. The flex layer is patterned and etched at 36 to form the supports and posts. In this embodiment the resistor network can be formed in the first or second metal layer, and the connections formed using the second or third metal layer. The resistors are formed in one metal layer and the connections made with a subsequent metal layer.

In yet another embodiment, a bus layer could be formed above the modulator elements. In this embodiment, a third sacrificial layer 38 is deposited and then a bus layer 40 deposited upon the third sacrificial layer. The bus layer is then patterned at etched at 42. Again, the resistors could be formed at 44, which may occur in one metal layer and connection provided at 46, in a subsequent metal layer. In the case of the bus layer embodiment, the resistors could be formed in the first, second or third metal layers, with the connections made using the second, third or fourth metal layers, so long as the connection layer is subsequent to the formation layer.

Having seen the individual resistor network, it is helpful to see a portion of an array with multiple lines as shown in Figure 6. The resistor networks 14a-d are connected to the outputs from the driver chips 50a-d. The shunt resistors R2a-d are connected to the

conductive bus line 18, with the output resistors R1a-d are connected to the modulator row lines, not shown, to provide the adjusted row voltage to the modulator elements. In this example, line 50d is active and the V_{pulse} is converted to V_{iMoD}.

In this manner, a standardized driver circuit such as an LCD driver chip can be used to drive other types of modulators through an adjuster circuit. The adjuster circuit provides stable, controlled output address voltage. As mentioned previously, it is also possible to apply this same modification to the column address pulses. The voltages and resistor values may vary, but a shunt resistor network applied to column addressing signals is within the scope of this invention.

Thus, although there has been described to this point a particular embodiment for a method and apparatus for a driver voltage adjustment, it is not intended that such specific references be considered as limitations upon the scope of this invention except in-so-far as set forth in the following claims.